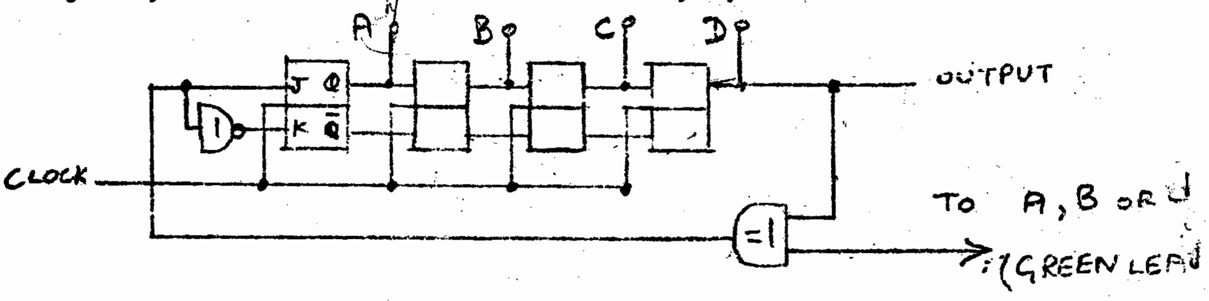
BBC ETD

PRELIMINARY PRACTICAL WORK SHEET

Psuedo-random Binary Generator

The circuit consists of a four stage shift register whose serial input is the output of an exclusive-OR gate. The inputs to this gate are the outputs of two of the bistables which form the register. One of these is wired to output D, the other can be connected to A, B, or C.



Connect this input to A, feed the clock input with a 10 kHz square wave and observe the output. It may be necessary to adjust the oscilloscope timebase vernier to obtain a stable display.

How many cycles of input elapse before the pattern is repeated?

Try to predict the pattern by considering the logic of the circuit. (Start with all bistables at logic '1'.)

What would happen if the bistables were all set to '0'? (This could happen on switch-on.)

Connect the flying lead to B. Observe the pattern.

How often does it repeat?

Is it possible for more than one pattern to be produced? Can you explain this?

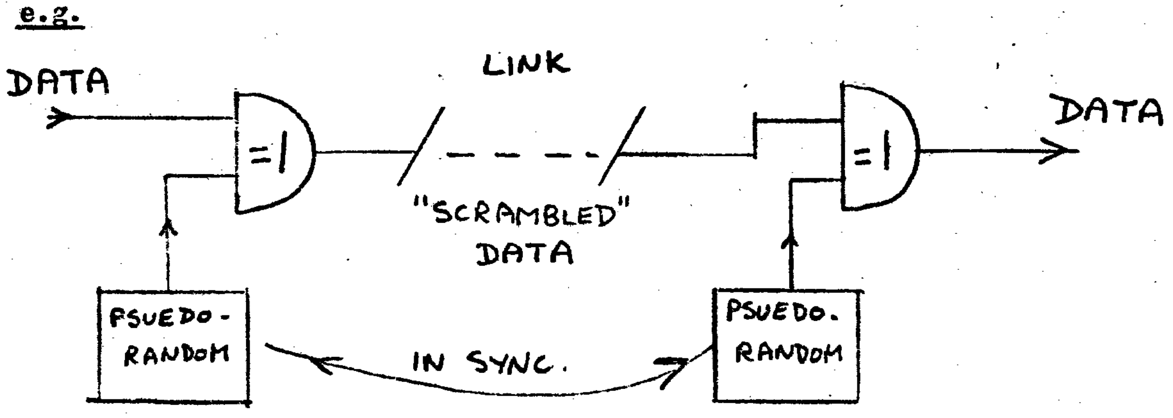
It would be quite easy to construct a generator of this type with, say, thirty stages. How often would the output pattern from this repeat?

Applications for this type of generator include;

1/ The testing of data links. (The waveform is random in nature but is predictable)

2/ The 'scrambling' of binary data for security purposes.

e.g.



If the random generators are the same, and are in synchronism, the apparently random signal on the link can be resolved at the receiving end.